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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|----------------------------|------------------|
| 10/762,445 | 01/22/2004 | Shenqing Fang | 0180192 | 3707 |
| 25700 | 7590 | 07/05/2005 | EXAMINER SARKAR, ASOK K | |
| FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691 | | | ART UNIT 2891 | PAPER NUMBER |

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|--------------------------------------|------------------------------------|--|
| Office Action Summary | Application No. 10/762,445 | Applicant(s) FANG ET AL. | |
| | Examiner Asok K. Sarkar | Art Unit 2891 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 6 and 8 – 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hori, US 6,147,379 in view of Kobayashi, US 6,721,205.

Regarding claims 1 and 8, Hori teaches a floating gate memory cell situated on a substrate, said floating gate memory cell comprising:

- a stacked gate structure 4 and 6 situated on said substrate 1, said stacked gate structure being situated over a channel region 9 in said substrate (see Fig. 1A);
- a recess 14 formed in said substrate adjacent to said stacked gate structure, said recess having a sidewall, a bottom, and a depth (see Fig. 1A);
- a source of said floating gate memory cell 7b situated adjacent to said sidewall of said recess and under said stacked gate structure (see Fig. 1A);
- a Vss connection region 7a situated under said bottom of said recess and under said source (see Fig. 1A), said Vss connection region being connected to said source, wherein said Vss connection region being situated under said bottom of said recess causes said source to have a reduced lateral diffusion in said channel region (this feature is inherent in Hori since the Vss connection is the bit line connection of the source through which is reference voltage Vs is applied

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during the operation of the memory cell) in between column 8, line 29 and column 9, line 23.

Hori shows the bit line connection in region 7a with reference to Fig. 1A, however, Kobayashi teaches that Vss connection region is the source of the memory cell through which the reference voltage is applied during the operation of the memory cell in column 19, lines 49 – 63.

Regarding claims 2 and 9, Hori teaches reduced lateral diffusion of source causing a reduction in drain induced barrier lowering in said floating gate memory cell since this feature will be inherent due to the structure of the memory cell as shown in Fig. 1A.

Regarding claims 3 and 10, Hori teaches the recess allows a resistance of said Vss connection region to be decreased without increasing drain induced barrier lowering in said floating gate memory cell as an inherent feature of the memory cell as shown in Fig. 1A.

Regarding claims 4 and 11, Hori teaches the sidewall of the recess is substantially perpendicular to a top surface of said substrate with reference to Fig. 1A.

Regarding claims 5 and 12, Hori teaches the depth of the recess is between approximately 200.0 Angstroms and approximately 500.0 Angstroms in column 8, lines 52 – 56.

Regarding claims 6 and 13, Hori teaches ONO stack situated on the floating gate in column 14, line 14.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Hori, US 6,147,379 in view of Kobayashi, US 6,721,205.

Hori fails to teach the floating gate memory cell is a NOR-type floating gate flash

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memory cell.

Kobayashi teaches that a memory cell comprising two impurity regions isolated from each other can be adopted for NOR type memory cell array in column 4, lines 17 – 25 for the benefit of reducing the DIBL effect in column 9, lines 7 – 11.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to use Hori's device in NOR type memory cell array for the benefit of reducing the DIBL effect as taught by Kobayashi in column 9, lines 7 – 11.

Conclusion

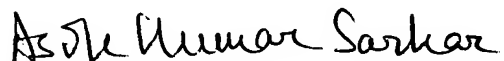
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Asok K. Sarkar
June 28, 2005

Primary Examiner